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Term: L5 same bus

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Search History

DATE: Wednesday, December 01, 2004 Printable Copy Create Case

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DB=USPT; PLUR=YES; OP=OR			
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DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L14	L13 same l2	3	L14
L13	logic adj1 design	4748	L13
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L11	L9 same l2	1	L11
L10	L9 same l7	1	L10
L9	exhaustive adj1 analysis	163	L9
L8	L7 same l2	40	L8
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L6	L5 and l1	1	L6
L5	L4 or l3	224	L5
L4	smallest adj1 cut	52	L4

L3	min-cut	173	L3
L2	tri-state near3 buses	1575	L2
L1	tri-state near3 bus	1575	L1

END OF SEARCH HISTORY

L18: Entry 2 of 3 File: USPT Apr 30, 1996

DOCUMENT-IDENTIFIER: US 5513124 A
TITLE: Logic placement using positionally asymmetrical partitioning method

Abstract Text (1):
A modified partitioning method for placement of a circuit design into a programmable integrated circuit device having a specific distribution of physical resources along a horizontal or vertical line in the device. The circuit design includes a plurality of circuit elements, for example three-state buffers which feed a common bus, or registers which receive a common clock signal. Such elements should or must be placed along a single horizontal or vertical line. One method includes the step of weighting connecting lines (nets) which join circuit elements to be placed along a common line with different weights for the horizontal and vertical directions. Alternatively, elements to be placed along the line are marked to be kept in line during partitioning. A min-cut algorithm then tends to or is required to avoid separating particular elements from a common line. The group containing the circuit elements with the line requirement is then partitioned such that the area and location of the group corresponds to the horizontal or vertical line.

Detailed Description Text (21):
The limitations of prior art min-cut algorithms are better understood with the following example of a three-state bus structure placed on a xilinx 4000-series FPGA.

Detailed Description Text (27):
Proper placement of a three-state bus structure is a particular problem with respect to placement-by-partitioning algorithms. Referring to the discussion above, the min-cut algorithm is not concerned with the orientation of associated elements, but only seeks to minimize the number of cut nets. Even the terminal propagation modification will not necessarily place Tbufs associated with a three-state bus structure on the same horizontal long line.

Detailed Description Text (30):
Assume that the partition line L1 is designated as "vertical". This would divide the resources of the simplified FPGA shown in FIG. 8 as indicated with line L1. The Tbufs T1-T4 of FIG. 7b would be placed to the left of line L1 in FIG. 8, and elements E1-E4 would be placed to the right of line L1. Note that there are 16 Tbufs located to the left of line L1, which would be recognized by the prior art min-cut algorithms as being sufficient to support the four Tbufs T1-T4 of FIG. 7b. What would not be recognized by the prior art min-cut algorithms is that only two of the 16 Tbufs to the left of line L1 are connected to any one of the eight long lines 43. Therefore, no subsequent partitions would result in a proper three-state bus structure wherein all four Tbufs T1-T4 would be connected to a common long line.

Detailed Description Text (31):
The same problem would eventually result if the first partition line is designated as horizontal, as indicated in FIG. 7c. This horizontal partition line is indicated in FIG. 8 as line L2. Line L2 divides the elements E1-E4 and Tbufs T1-T4 such that it appears the Tbufs could be connected to a common long line. The prior art min-

cut algorithm would then attempt to partition the Tbufs T1-T4 with partition line L3, shown in FIG. 7d. Because the next partition line would be designated as vertical, the Tbufs would be divided as shown in FIG. 7d into a group containing T1 and T2, and a group containing T3 and T4. At this point it is still possible to combine the four Tbufs such that they are connected to a single long line because the line L3 (shown in FIG. 8) divides the four Tbufs and does not preclude connecting the four Tbufs to a long line located above line L1. However, because the min-cut algorithm has not reached a stop condition, the two groups of Tbufs would be further partitioned. Because the next partition lines L4 and L5 would be designated as horizontal, the Tbufs would be divided as shown in FIG. 7e, such that two of the Tbufs T1 and T3 are placed in the top two rows of Tbufs (shown in FIG. 8), and two of the Tbufs T2 and T4 are placed in the second two rows of Tbufs. Because this occurs, the prior art min-cut algorithms fail to place the Tbufs such that a proper three-state bus structure is formed.

Detailed Description Text (41):
In a third embodiment, useful when specific circuit elements must be grouped on a single horizontal or vertical line, cells are not formed as in the first embodiment, and weights are not assigned as in the second embodiment. Instead, particular lines in the design (nets) are identified as having a constraint, namely being connected to a named line. In the Tbuf example, the net which is to serve as a bus is so marked. During min-cut partitioning, when one element which connects to a bus is separated from the others by a horizontal cut line, all other elements connected to the common bus are moved across the cut line. Thus all elements connected to a bus are moved together during min-cut partitioning. In the common clock example, the clock line is so marked and elements to be driven from this common clock line are moved together across a vertical cut line. It may be preferred not to mark elements which are preferably but not necessarily aligned vertically, since so marking will significantly restrict the placement freedom.

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L18: Entry 3 of 3 File: USPT Jun 29, 1993

DOCUMENT-IDENTIFIER: US 5224056 A
**** See image for Certificate of Correction ****
TITLE: Logic placement using positionally asymmetrical partitioning algorithm

Detailed Description Text (21):
The limitations of prior art Min-cut algorithms are better understood with the following example of a three-state bus structure placed on a Xilinx 4000-series FPGA.

Detailed Description Text (27):
Proper placement of a three-state bus structure is a particular problem with respect to placement-by-partitioning algorithms. Referring to the discussion above, the Min-cut algorithm is not concerned with the orientation of associated elements, but only seeks to minimize the number of cut nets. Even using the terminal propagation modification, the associated Tbufs of a circuit design containing a three-state bus structure can be placed such that they are not connected to the same horizontal long line.

Detailed Description Text (30):
Assume that the partition line L1 is designated as "vertical". This would divide the resources of the simplified FPGA shown in FIG. 8 as indicated with line L1. The Tbufs T1-T4 of FIG. 7b would be placed to the left of line L1 in FIG. 8, and elements E1-E4 would be placed to the right of line L1. Note that there are 16 Tbufs located to the left of line L1, which would be recognized by the prior art Min-cut algorithms as being sufficient to support the four Tbufs T1-T4 of FIG. 7b. What would not be recognized by the prior art Min-cut algorithms is that only two of the 16 Tbufs to the left of line L1 are connected to any one of the eight long lines 43. Therefore, no subsequent partitions would result in a proper three-state bus structure wherein all four Tbufs T1-T4 would be connected to a common long line.

Detailed Description Text (31):
The same problem would eventually result if the first partition line is designated as horizontal, as indicated in FIG. 7c. This horizontal partition line is indicated in FIG. 8 as line L2. Line L2 divides the elements E1-E4 and Tbufs T1-T4 such that it appears the Tbufs could be connected to a common long line. The prior art Min-cut algorithm would then attempt to partition the Tbufs T1-T4 with partition line L3, shown in FIG. 7d. Because the next partition line would be designated as vertical, the Tbufs would be divided as shown in FIG. 7d into a group containing T1 and T2, and a group containing T3 and T4. At this point it is still possible to combine the four Tbufs such that they are connected to a single long line because the line L3 (shown in FIG. 8) divides the four Tbufs and does not preclude connecting the four Tbufs to a long line located above line L1. However, because the Min-cut algorithm has not reached a stop condition, the two groups of Tbufs would be further partitioned. Because the next partition lines L4 and L5 would be designated as horizontal, the Tbufs would be divided as shown in FIG. 7e, such that two of the Tubfs T1 and T3 are placed in the top two rows of Tbufs (shown in FIG. 8), and two of the Tbufs T2 and T4 are placed in the second two rows of Tbufs.

Because this occurs, the prior art Min-cut algorithms fail to place the Tbufs such that a proper three-state bus structure is formed.

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